## ABSTRACT OF THE DISCLOSURE

A bridge accessible by a host processor can expand access over a first bus to a second bus. The first bus and the second bus are each adapted to separately connect to respective ones of a plurality of bus-compatible devices. Allowable ones of the devices include memory devices and input/output devices. The bridge has a link, together with a first and a second interface. The first interface is coupled between the first bus and the link. The second interface is coupled between the second bus and the link. The first interface and the second interface are operable to (a) send information serially through the link in a format different from that of the first bus and the second bus, (b) approve an initial exchange between the first bus and the second bus in response to pending transactions having a characteristic signifying a destination across the bridge, (c) exchange information between the first bus and the second bus according to a predetermined hierarchy giving the first bus a higher level than the second bus, and (d) allow the host processor, communicating through the first bus, to individually address different selectable ones of the bus-compatible devices on the second bus, including memory devices and input/output devices that may be present: (i) using on the first bus substantially the same type of addressing as is used to access devices the first bus, and (ii) without first employing a second, intervening one of the bus-compatible devices on the second bus.